BSPDN-Elite: A Comprehensive Framework for Optimizing Timing, Power and Routing Resources in BSPDN Designs

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Abstract

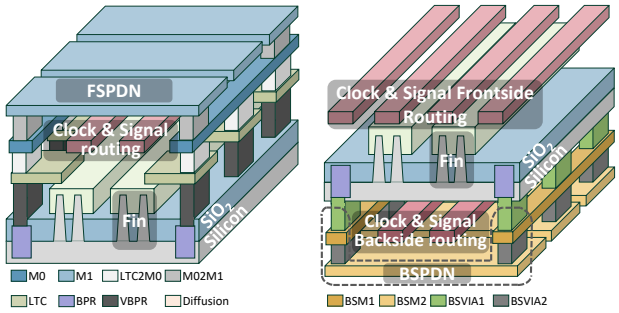
Backside power delivery networks (BSPDN) provide superior power integrity while freeing backside routing resources. However, existing works fail to fully exploit these resources for power, performance, and area (PPA) optimization through strategic net allocation. This paper presents a co-optimization framework that maximizes PPA by strategically routing both clock and signal nets on the backside, enabling double-side routing. Experimental results demonstrate 88.1% IR-drop reduction, 23.0% frequency improvement, 10.9% power savings, and timing improvements (66.3% WNS, 40.2% TNS) over FSPDN with negligible nTSVs overhead.

1 Introduction

The semiconductor industry faces a critical inflection point at sub-3nm nodes, where traditional front-side PDN (FSPDN) designs have reached their fundamental physical limits. Increasing metal resistance coupled with unprecedented current demands has created catastrophic IR-drop scenarios that threaten performance [1, 2]. This challenge is exacerbated by the competition between power delivery and signal routing in conventional designs. Backside power delivery networks (BSPDN) have emerged as a revolutionary paradigm shift to address these challenges [3, 4]. As illustrated in Figure 1, by relocating power distribution to the chip's backside via nano-through-silicon vias (nTSVs), BSPDN significantly mitigates IR-drop while liberating frontside routing resources for double-side routing, achieving substantial power efficiency gains [5–8].

While BSPDN liberates valuable backside routing resources, existing approaches face critical limitations in resource utilization. Clock-centric strategies [9, 10] relocate clock networks to the backside but neglect timing-critical signal paths, leaving potential performance gains unrealized. Conversely, signal-centric methods [11–14] migrate signal nets based on geometric criteria (bounding box size, pin count, or congestion metrics) but fail to prioritize timing-critical paths, as geometric size poorly correlates with path slack. Moreover, both approaches overlook a fundamental challenge: the elimination of frontside PDN structures removes electromagnetic shielding traditionally provided by P/G (power/ground) grids, introducing severe signal integrity (SI) degradation [15, 16].

This paper presents a comprehensive framework for maximizing PPA benefits in BSPDN designs through strategic co-optimization of both clock and signal nets. Our contributions are as follows:



(a) FSPDN (b) BSPDN

Figure 1: Cross-section views of conventional FSPDN with frontside routing vs. BSPDN with double-side routing.

- We developed a comprehensive co-optimization flow integrating net selection, placement adjustment, and BSPDN refinement.
- We developed an importance-weighted graph classification method for double-side routing selection that addresses signal integrity issues by leveraging PDN structures as natural shields.
- We pioneered backside-aware cell placement techniques that reposition driver and load cells to minimize Design Rule Check (DRC) violations and improve routing quality.
- We developed adaptive BSPDN refinement that fills remaining backside resources with power stripes to reduce IR-drop.

2 Preliminaries

2.1 BSPDN Structure

With scaling beyond 5*nm*, conventional FSPDN designs face critical challenges. As shown in Figure 1(a), increased metal resistance causes severe IR-drop, while higher transistor density and routing congestion force designers to compromise between power integrity and signal routability [2]. BSPDN addresses these challenges by relocating power distribution to the chip's backside [17, 18]. As shown in Figure 1(b), BSPDN utilizes wide, thick metal layers with lower resistivity, substantially reducing IR-drop [3]. nTSVs with diameters below 100*nm* connect backside metal to frontside buried power rails, delivering power while freeing frontside routing resources [19, 20].

2.2 Related Works

After establishing BSPDN, significant routing resources remain available. Existing research explores two main approaches with notable limitations:

Clock-Specific Routing: This approach relocates clock networks to the backside using specialized backside buffer cells (BSBUF) with integrated nTSVs [9, 10, 16, 17]. GNN-based endpoint classification algorithms select clock trunk signals for backside placement,

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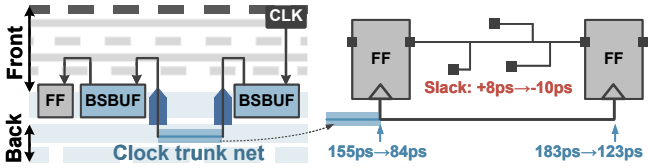


Figure 2: Backside clock routing reduces latency but degrades setup margins. Example: 90% BSPDN utilization increases skew from 28 ps to 39 ps.

Table 1: Performance comparison of frontside vs. backside clock tree in SHA256 design (frontside: M0-M6; backside: BSM1-BSM3).

Metrics	FSPDN	BSPDN		
		Backside PDN Utilization		
		30%	70%	90%
Clock Skew (ps)	28	9	15	39
Clock Latency (ps)	183	87	105	123
WNS (ps)	**-199**	-177	**-209**	**-219**
TNS (ns)	**-4.1**	-3.2	**-4.0**	**-4.2**
IR-drop (mV)	36.71	11.83	8.76	3.34

demonstrating improvements in clock skew and latency [9]. However, these approaches neglect critical signal paths, creating suboptimal results when timing-critical nets remain frontside-constrained.

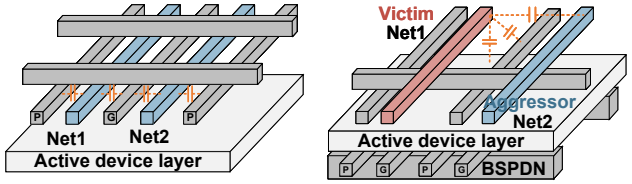
Geometric-based Signal Routing: These methods select nets based on bounding box size, pin count, or congestion metrics to improve routability [11–14]. However, geometric criteria fail to accurately identify critical timing paths, as they lack direct correlation with path slack or criticality. A net with a small bounding box can still be on the critical path, while a geometrically large net may have substantial slack. This fundamental limitation prevents geometric methods from achieving optimal timing-driven backside allocation. Moreover, treating clock and signal optimization as separate problems ignores their interdependent effects, necessitating a comprehensive co-optimization framework.

3 Motivations

Despite its transformative potential, BSPDN design faces three critical implementation challenges that motivate our methodology.

❶ **Clock-signal interdependency** necessitates co-optimization rather than isolated approaches. As illustrated in Figure 2, backside clock optimization achieves significant clock latency reduction from 183 ps to 123 ps. However, this improvement comes at the cost of dramatically tightened clock skew, decreasing from 28 ps to merely 39 ps. Consequently, the data path slack degrades from a positive 8 ps margin to a critical -10 ps setup violation for signal nets that remain on the frontside. Table 1 quantifies this fundamental trade-off: while backside clocking substantially reduces IR-drop and improves clock latency, WNS deteriorates at high PDN utilization. Specifically, at 70% and 90% utilization, WNS degrades to -209 ps and -219 ps respectively, worse than the baseline FSPDN at -199 ps. This motivates our **importance-weighted graph classification framework** (Section 4.1) for unified multi-criteria evaluation of both clock and signal nets.

❷ **Signal integrity degradation** emerges due to eliminating frontside PDN shielding. Conventional FSPDN uses P/G grids as natural shields between signal nets, as illustrated in Figure 3. The metal strips of P/G networks effectively isolate signal routing, substantially attenuating capacitive coupling. BSPDN removes this shielding in Figure 3(b), enhancing direct coupling between victim (Net1, red) and aggressor nets (Net2, blue). This drives our **post-implementation SI refinement** strategy (Section 4.1) that allocates SI-sensitive nets to the backside to leverage BSPDN P/G strips for crosstalk shielding.



(a) FSPDN + FS Routing (b) BSPDN + FS Routing

Figure 3: SI degradation: (a) FSPDN's P/G shielding suppresses crosstalk; (b) BSPDN removes shielding, increasing coupling.

❸ **Physical constraints in double-side routing** present resource allocation challenges. nTSV placement introduces DRC constraints with area/timing penalties. Furthermore, physical conflicts between nTSV and PDN can displace clock buffers up to 4.13 µm at 70% BSPDN utilization [16]. Limited backside metal resources create conflicting allocation demands among power, clock, and signal nets. This motivates our **backside-aware cell placement adjustment** (Section 4.2) and **dynamic backside resource allocation** (Section 4.3) with adaptive segmented PDN stripes.

4 Methodology

We present a framework for maximizing double-side routing benefits through three components: (1) importance-weighted net selection for double-side routing; (2) backside-aware cell placement optimization; and (3) adaptive PDN stripe refinement. These components form an integrated flow where net selection guides placement adjustment, enabling subsequent PDN optimization.

4.1 Importance-Weighted Graph Classification for Double-side Net Allocation

Our methodology implements a graph-based net classification strategy that identifies promising candidates for double-side routing migration. Unlike conventional circuit graphs that model cells as nodes and nets as edges, we construct an line graph where nets become nodes and cells define connectivity, enabling more effective analysis of net interaction patterns for migration decisions.

Inverted Circuit-to-Graph Transformation: We construct a line graph $G_{\text{net}} = (V_{\text{net}}, E_{\text{cell}})$ where each net n_i becomes a vertex v_i (circles in Figure 4), and cells connecting multiple nets define edges between vertices. Unlike conventional circuit graphs that model cells as nodes, this inversion enables: (1) nets with strong functional relationships form densely connected subgraphs; (2) vertex neighborhoods reveal migration impact on surrounding design regions; (3) natural separation of clock (darker vertices) and signal (lighter vertices) communities emerges. Each vertex v_i is annotated with attributes from post-route timing analysis: number of loads (N_{loads}), timing path statistics (T_{crit}, T_{all}), total capacitance (C_{total}), and signal type classification. Edge weights capture functional connectivity strength based on shared cell instances.

Importance-Weighted Net Classification: Net selection is formulated as a vertex classification task: identifying which vertices (solid circles in Figure 4) should migrate to the backside while others (hollow circles) remain on the frontside. We define empirically-derived importance functions for different vertex categories based

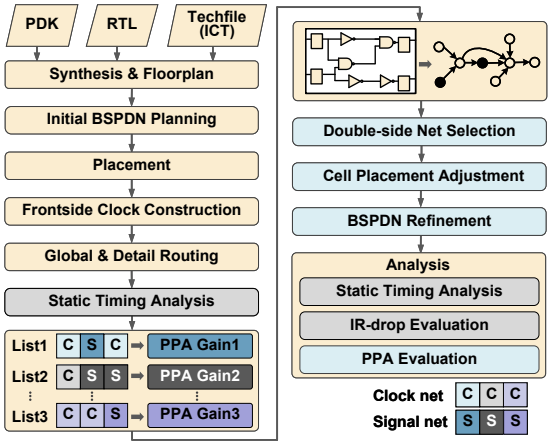


Figure 4: Overview of the proposed BSPDN-Elite flow.

on post-route timing analysis. For clock net vertices, we prioritize high-fanout nets closer to clock roots:

$$W_{\text{clock}}(v_i) = \frac{N_{\text{loads}} \cdot C_{\text{total}}}{\ln(P_{\text{clk}} + 1)}, \tag{1}$$

where P_{clk} represents the clock hierarchy level (distance from clock source), with lower values indicating higher criticality and greater timing impact. For signal net vertices, we emphasize timing path criticality and net complexity:

$$W_{\text{signal}}(v_i) = \frac{N_{\text{loads}} \cdot [\lambda \cdot T_{\text{all}} + (1-\lambda) \cdot T_{\text{crit}}] \cdot C_{\text{total}}}{\ln(P_{\text{path}} + 1)}, \tag{2}$$

where T_{all} and T_{crit} count the total number of timing paths and critical paths (slack < 0) passing through the net, respectively. P_{path} represents the criticality rank of the net's worst slack in the global timing path list, with lower values indicating more severe timing violations. The empirical balancing factor $\lambda = 0.5$ weighs path quantity against individual path criticality. The capacitance term C_{total} prioritizes high-capacitance nets where double-side routing can reduce wire delay through shorter, less congested routing paths.

Multi-Configuration Exploration: We systematically explore multiple classification strategies through diverse net lists. As shown in Figure 4, List1 ("C, S, C"), List2 ("C, S, S"), and List3 ("C, C, S") represent different clock-to-signal ratios and threshold variations. Each configuration undergoes full implementation with evaluation of timing improvements (WNS/TNS), nTSV implementation cost, power efficiency, and IR-drop performance.

Post-Implementation SI Refinement: Following initial double-side routing, we perform targeted signal integrity enhancement. Eliminating frontside PDN structures removes electromagnetic shielding previously provided by P/G grids [15, 16], increasing crosstalk between adjacent nets. Post-routing SI analysis identifies nets with voltage bump or delta delay ratios exceeding 40%. These SI-sensitive nets migrate to backside layers where BSPDN P/G strips provide shielding, independent of initial classification. This decoupled SI optimization proves more resource-efficient than extending backside power structures frontside, as SI degradation correlates with routing density rather than timing metrics. The final classification (Clock: "C, C, C", Signal: "S, S, S") with SI refinements feeds into subsequent placement adjustment and BSPDN utilization stages.

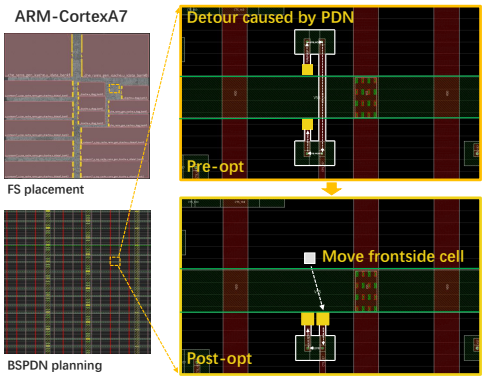


Figure 5: Cell adjustment showing initial placement and optimized placement.

Algorithm 1 : Backside-aware Cell Placement Optimization

Input : Selected backside nets $\mathcal{N}_{BS}$, Backside PDN placement $\mathcal{P}_{BS}$, Cell max displacement d_{max}
Output : Optimized cell positions

```
// Step 1: Identify PDN-constrained regions
R_PDN ← ExtractPDNFootprint(P_BS);
// Step 2: Incremental cell adjustment
foreach net n ∈ N_BS do
    foreach cell c in drivers/loads of n do
        candidates ← GenerateLegalPositions(c, d_max);
        candidates ← FilterPDNConflicts(candidates, R_PDN);
        best_pos ← argmax_p Score(c, p);
        if Score(c, best_pos) > Score(c, current_pos) then
            MoveCell(c, best_pos);
return Updated cell positions;
```

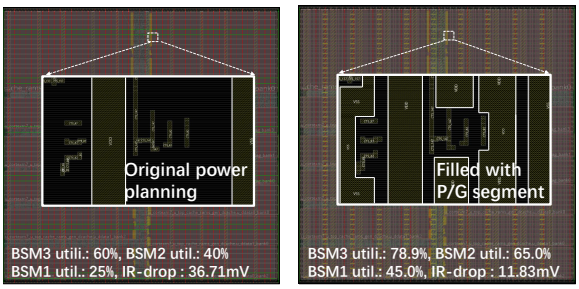
4.2 Backside-Aware Placement Optimization

After identifying candidate nets for double-side routing, the backside PDN structures occupy significant routing space, potentially blocking optimal signal paths. We perform localized cell placement adjustments to improve double-side routing quality while avoiding PDN conflicts. Figure 5 illustrates the core challenge and our solution. In the pre-optimization state (top), driver and load cells are positioned without considering backside PDN layout, forcing routing paths to detour around PDN stripes. By strategically moving frontside cells (bottom), we create cleaner backside routing channels that avoid PDN blockages.

We first extract the footprint of backside PDN structures from the physical layout, identifying regions where signal routing is prohibited or discouraged. For each selected net, we evaluate small perturbations to driver/load cell positions. Each candidate position is scored based on:

$$Score(p) = w_T \cdot \Delta Timing(p) - w_D \cdot Distance(p), \tag{3}$$

where $\Delta Timing(p)$ estimates timing impact and $Distance(p)$ measures displacement from the original position. Movement is constrained to 5-10 standard cell widths to maintain placement stability. The weights w_T and w_D are empirically set to 0.5 and 0.5, respectively. Positions that conflict with PDN regions are filtered out during candidate generation, ensuring all evaluated positions are legally routable. We apply a greedy optimization approach that



(a) Initial uniform BSPDN planning (b) Post-optimized BSPDN

Figure 6: BSPDN refinement: (a) Initial uniform PDN and (b) enhanced PDN with segmented stripes.

iterates through all nets in the candidate set, as detailed in Algorithm 1. For each net, we evaluate driver and load cell movements independently, accepting improvements that increase the overall score. The optimization proceeds in multiple passes over the net list, with each pass potentially finding new improvement opportunities as cells are repositioned. The process continues until no further score improvements can be found across all nets or a maximum iteration limit is reached to prevent excessive runtime. This greedy strategy provides a good balance between solution quality and computational efficiency, avoiding the exponential complexity of exhaustive position search while still achieving significant routing quality improvements. By incrementally repositioning cells to align with available backside routing channels, we reduce wire detours around PDN structures and improve both wire length and timing metrics for backside-routed nets.

4.3 BSPDN Refinement

Following backside clock and signal routing, we fill underutilized regions with supplementary PDN segments. This step is particularly challenging in our work compared to prior work [16], as we must navigate around both clock and signal routing rather than clock nets alone. Figure 6 illustrates our BSPDN refinement approach, comparing (a) the initial uniform PDN allocation with (b) the optimized configuration that employs segmented stripes to fill available space while accommodating critical signal routing. We implement two refinement strategies:

(1) **Available space detection**: We analyze the occupancy maps of BSM1 and BSM2 layers generated from previous routing stages. For each layer, we identify maximal rectangular regions bounded by existing metal structures (clock routes, signal nets, and initial PDN straps) that satisfy minimum dimension requirements for PDN segments. A region qualifies if it satisfies: (i) minimum dimensions (2-3× metal width), (ii) clearance from adjacent routing, and (iii) alignment with existing straps for connectivity, critical given the irregular fragmentation from dense backside signal routing.

(2) **Segment generation**: Within each identified available region, we insert P/G segments using a greedy space-filling strategy based on the Innovus `trim_pg` command. For regions where the gap between consecutive occupied areas exceeds the unit pitch (defined as target width plus spacing), we calculate the maximum number of segments that can fit: $N = \lceil (\text{gap\_length} - 2 \times \text{spacing}) / (\text{width} + \text{spacing}) \rceil$, where gap_length is the distance between adjacent blockages. Each segment's height spans the unoccupied region between adjacent routing blockages in the orthogonal direction. This adaptive approach naturally accommodates irregular routing patterns and varying gap sizes across the backside metal layers.

The space search operates in a greedy manner, prioritizing larger available regions and areas with higher IR-drop. For BSM1 (horizontal PDN), we scan row-by-row to identify gaps between existing structures. For BSM2 (vertical PDN), we perform column-wise scanning. Each candidate region is validated against design rules before segment insertion. This fill-based approach maximizes utilization of otherwise wasted backside resources without requiring complex track reallocation or routing rip-up. By inserting segments only in genuinely available space, we avoid conflicts with previously routed critical signals while opportunistically improving power delivery where resources permit.

Table 2: Technology specifications and design rules.

Backside	Width/ Spacing (μm)	Pitch (μm)	Frontside	Width/ Spacing (μm)	Pitch (μm)
BSM0	0.053 / 0.028	0.04	M0	0.020 / 0.020	0.04
BSM1	0.125 / 0.375	0.5	M1	0.037 / 0.020	0.06
BSM2	0.5 / 1.5	2	M2/3	0.020 / 0.020	0.04
BSM3	0.5 / 1.5	2	M4/5/6/7/8/9	0.038 / 0.038	0.08

5 Experimental Results

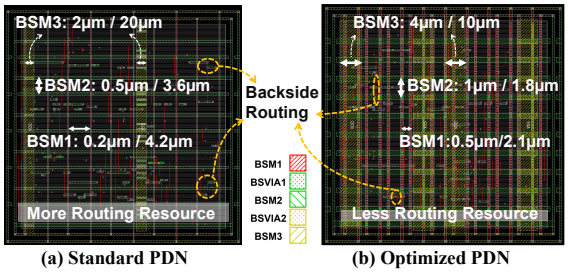
5.1 Experimental Setup

Our BSPDN implementation utilizes nTSVs to establish electrical connections between local buried power rails (BPRs) and backside metal layers [3]. The metal layer configuration follows the parameters in Table 2. We evaluate benchmark designs including SHA256, JPEG [21], and ARM Cortex-A7 [22]. All designs are implemented in a commercial 7*nm* library (VDD = 0.75V, TT Corner) using Cadence Genus [23] for synthesis and Innovus [24] for place-and-route. Power integrity analysis employs an in-house IR-drop tool [2], and sign-off timing uses Synopsys PrimeTime SI [25] with back-annotated parasitics.

To determine the optimal PDN configuration, we compare standard uniform BSPDN (Std. BSPDN) with an optimized version (Opt. BSPDN) featuring enhanced dimensions. As shown in Figure 7, Opt. BSPDN doubles BSM3 width (2 to 4 μm) and halves pitch (20 to 10 μm) versus Std. BSPDN. The approach was implemented in Python 3.8.5 on Rocky Linux 8 with dual Intel Xeon Platinum 8480+ (112 cores) and two NVIDIA L40S GPUs (46GB each).

5.2 PPA and IR-drop Evaluations

Table 3 demonstrates our three-stage optimization benefits. Compared to conventional FSPDN, our optimized BSPDN achieves 23.0%



(a) Standard PDN (b) Optimized PDN

Figure 7: Comparative BSPDN stripe configurations: Standard BSPDN (Std. BSPDN) vs. Optimized BSPDN (Opt. BSPDN). Opt. BSPDN features a denser power grid with improved IR-drop.

Table 3: Metrics comparison between FSPDN and BSPDN variants across three benchmarks. All BSPDN designs use Opt. BSPDN configuration shown in Figure 7(b).

Metrics	SHA256 (#Cell = 7.9k)					JPEG (#Cell = 182k)					ARM Cortex-A7 (#Cell = 108k)				
	FSPDN+ FS Routing	BSPDN+ FS Routing	DAC24 [9]	DAC25 [16]	Ours	FSPDN+ FS Routing	BSPDN+ FS Routing	DAC24 [9]	DAC25 [16]	Ours	FSPDN+ FS Routing	BSPDN+ FS Routing	DAC24 [9]	DAC25 [16]	Ours
Eff. Freq (GHz)	1.50	1.64	1.70	1.65	**2.05**	1.54	1.61	1.63	1.71	**1.84**	1.78	1.83	1.89	1.91	**2.04**
Utilization (%)	82.91	82.36				78.24	65.50				78.16	74.15			
Area (μm^2)	1319	1311				32280	31285				14267	13491			
#Metal (BS+FS)	0+6	3+6				0+7	3+7				0+8	3+8			
#nTSVs	-	-	270	194	248	-	-	396	768	800	-	-	316	634	676
Max. Disp. (μm)	-	-	-	1.78	2.37	-	-	-	4.69	3.21	-	-	-	5.78	6.46
Clock Skew (ps)	24.17	27.94	27.02	26.56	27.01	112.16	35.3	31.9	29.87	32.67	217.67	95.06	66.79	61.76	64.56
Clock Latency (ps)	83.29	75.31	64.63	60.11	65.37	226.26	149.31	112.11	109.89	112.48	456.98	206.51	147.67	136.78	138.97
Wirelength (m)	0.048	0.038	0.037	0.036	0.037	0.81	0.70	0.69	0.68	0.68	1.47	1.37	1.38	1.38	1.40
Total Power (mW)	7.41	7.17	6.77	7.09	**5.63**	152.92	143.42	149.01	135.36	**134.28**	140.97	131.93	133.67	131.67	**128.56**
WNS (ns)	-0.196	-0.111	-0.094	-0.106	**-0.076**	-0.126	-0.122	-0.125	-0.098	**-0.057**	-0.194	-0.081	-0.092	-0.099	**-0.040**
TNS (ns)	-4.06	-1.96	-2.04	-2.14	**-1.69**	-28.53	-25.25	-24.44	-25.06	**-17.95**	-1.756	-1.637	-1.5797	-1.058	**-0.9245**
IR-drop (mV)	36.71	14.53	14.72	10.79	**10.71**	55.95	16.06	16.11	11.56	**10.72**	170.02	18.93	15.78	15.67	**9.76**

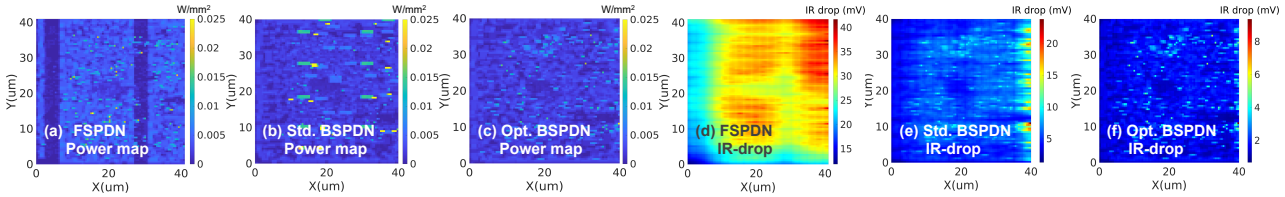


Figure 8: Power density maps and IR drop heatmaps: (a-c) Power density distribution for FSPDN, standard BSPDN, and optimized BSPDN showing progressive improvement in power delivery uniformity; (d-f) Corresponding IR drop heatmaps demonstrating significant voltage drop reduction from FSPDN to Opt. BSPDN.

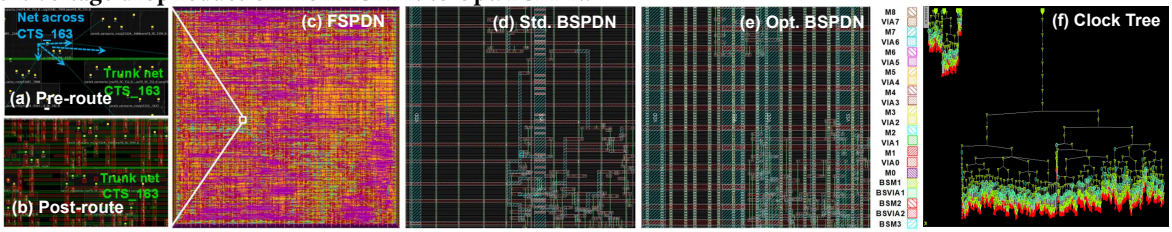


Figure 9: Routing comparison on JPEG: (a-b) Clock trunk net `CTS_163` resource contention before and after optimization; (c) Conventional FSPDN with frontside-only routing; (d) Standard BSPDN with uniform PDN; (e) Optimized BSPDN with dynamic resource allocation; (f) Complete clock tree structure.

higher effective frequency (averaged: 1.98 GHz vs 1.61 GHz), 10.9% power reduction, 66.3% WNS improvement, 40.2% TNS improvement, and 88.1% IR-drop reduction. These gains stem from our integrated methodology: importance-weighted graph classification identifies high-impact nets for backside migration by prioritizing high-fanout, timing-critical paths where double-side routing maximizes benefit. This selective strategy allocates backside resources to nets genuinely benefiting from reduced congestion, rather than indiscriminate migration. Backside-aware cell placement then optimizes driver/load positions to minimize PDN-induced detours, improving wire length and timing. Finally, adaptive BSPDN refinement fills remaining resources with segmented PDN stripes, delivering exceptional IR-drop reduction while preserving routing channels for migrated signals.

However, our approach involves deliberate trade-offs. While clock skew metrics (27.01 ps for SHA256) are competitive, they are slightly higher than the state-of-the-art DAC'25 [10] (27.01 ps vs 26.56 ps, +1.7%). This modest difference reflects our holistic design philosophy: rather than exclusively optimizing clock distribution, our importance-weighted net selection balances clock nets against critical signal paths, and our BSPDN refinement allocates backside resources to both routing and power delivery. This design philosophy delivers superior overall design quality, as our 88.1% IR-drop reduction and 10.9% power savings outperform clock-centric approaches that sacrifice PDN performance for marginal skew improvements. The maximum cell displacement increases with design complexity (SHA256: 2.37 µm, JPEG: 3.21 µm, ARM: 6.46 µm), as larger designs require more aggressive placement perturbations to navigate backside PDN constraints. However, all displacements remain within 5-10 standard cell widths, maintaining placement stability.

Figure 8 visualizes the progressive IR-drop improvements enabled by our methodology. FSPDN suffers severe voltage drop (36.71 mV worst-case) due to limited frontside PDN resources competing with dense signal routing. Standard BSPDN with uniform backside PDN allocation reduces IR-drop to 22 mV but wastes resources in lightly loaded regions. Our optimized solution achieves 10.71 mV worst-case IR-drop through the adaptive BSPDN refinement by filling available backside regions with segmented stripes; after critical signal routing, we maximize power delivery density in high-demand

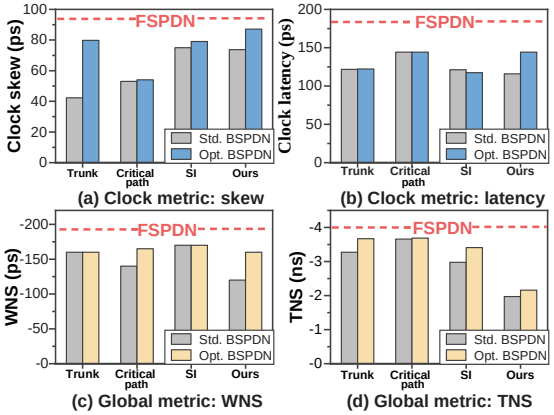


Figure 10: Comparison of metrics across net selection strategies with Std. BSPDN and Opt. BSPDN.

areas while avoiding unnecessary blockages in others. Figure 9 illustrates the routing evolution that enables these improvements. The pre-route and post-route comparisons in Figure 9(a-b) show how clock trunk net `CTS_163` competes with numerous signal nets for frontside resources. Our graph-based classification identifies such high-fanout clock nets as prime backside candidates. The full-chip layouts in Figure 9(c-e) demonstrate the architectural progression: conventional FSPDN exhibits severe routing congestion, standard BSPDN with uniform PDN wastes backside capacity, while our optimized design employs the segmented PDN strategy to balance signal routing with power delivery. The complete clock tree structure in Figure 9(f) confirms that strategic backside migration successfully relieves frontside pressure while maintaining clock quality, demonstrating how our framework strategically utilizes double-side resources for PPA improvement.

5.3 Net Selection Strategy Comparison

To validate our importance-weighted methodology, we compare four net selection strategies under identical BSPDN infrastructure (Std. and Opt. BSPDN). As shown in Figure 10: (1) **Trunk** prioritizes high-fanout clock nets via N_{loads} and C_{total}; (2) **Critical path** emphasizes nets with highest criticality rank P_{path}; (3) **SI** migrates nets with delta delay or voltage bump ratios exceeding 30%; (4) **Ours** integrates hybrid weighting with multi-configuration exploration and SI refinement. **Single-objective strategies show limited coverage.** Trunk excels in clock metrics (43.75% skew reduction: 95→55 ps, 25% latency improvement) but provides minimal global timing benefits (WNS: -165 ps, TNS: -3.6 ns). Conversely, Critical path improves WNS/TNS but degrades clock quality, while SI addresses crosstalk but misses timing-critical nets without severe violations. **Our hybrid approach unifies complementary objectives.** Integrating clock-centric weighting, signal net balancing, and SI refinement, our methodology achieves superior performance: 10% better WNS than Critical path, 30% better skew than SI, and 15% TNS improvement over Trunk. Figure 11 demonstrates SI refinement effectiveness: backside P/G shielding reduces delta delay from 160 ps to <1 ps, while eye diagrams show width expanding from 15% to 95% and height from 23% to 97%.

PDN configuration impact. Comparing Std. versus Opt. BSPDN, the optimized PDN provides 8-12% additional headroom across all strategies. However, relative rankings remain unchanged, confirming our methodology's advantages stem from intelligent net prioritization rather than PDN density alone.

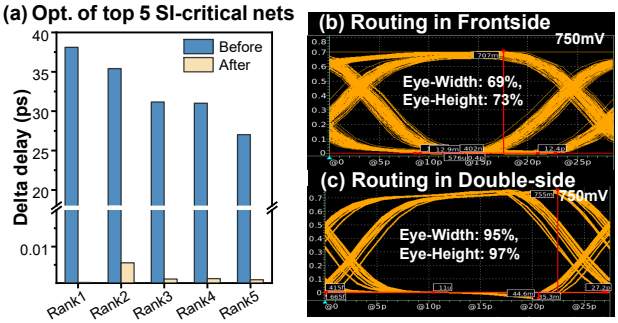


Figure 11: SI improvement: (a) delta delay reduction across top-5 critical nets; eye diagram showing (b) frontside routing degradation and (c) double-side routing recovery.

Table 4: Ablation study using Opt. BSPDN.

Configuration	Full Method	w/o BSPDN Refine.	w/o Place. & Refine.	w/o Net Select.
Freq. Improv. (%)	**+23.6**	+21.3	+18.5	+8.2
Power Reduct. (%)	**-15.0**	-13.7	-11.8	-5.1
Area Reduct. (%)	**-3.0**	-1.5	0	0
IR-drop Reduct. (%)	**-82.0**	-78.6	-65.3	-62.4

5.4 Ablation Studies

To evaluate each component's contribution, we conducted ablation experiments. Table 4 demonstrates that all three components synergistically contribute to overall performance, with improvements measured relative to the FSPDN+FS Routing baseline.

Net Selection (§4.1) provides the foundational optimization, contributing the primary improvements in frequency (+8.2%), power (-5.1%), and IR-drop (-62.4%). The importance-weighted graph classification with multi-configuration exploration effectively identifies optimal candidates for backside migration.

Placement Adjustment (§4.2) contributes additional gains by enabling PDN-aware cell repositioning. This component enhances frequency by 10.3% and power by 6.7%, validating the importance of placement-routing co-optimization in backside-aware design.

BSPDN Refinement (§4.3) adds the final increment through opportunistic space filling with PDN segments. While contributing smaller percentage gains in frequency and power, this component proves critical for maximizing IR-drop reduction (from -65.3% to -82.0%) and achieving area savings through efficient resource utilization.

6 Conclusion

This paper introduces a comprehensive double-side routing methodology for BSPDN designs with three integrated optimization stages: pre-routing net selection, backside-aware cell placement adjustment, and dynamic backside resource allocation. Experimental results demonstrate significant PPA improvements compared to conventional methods, successfully navigating the complex trade-offs in double-side routing while preserving the power delivery advantages of BSPDN for next-generation 3D ICs.

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